MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Quarterly Report #7

(Contract NIH-NINDS-NO1-NS-9-2304)

October – December 2000

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

by the

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48109-2122

January 2001

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400μm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters.

During the past quarter, work has progressed in several areas. Additional STIM-2B/-3B probes were processed to completion. Several of the STIM-2B probes were mounted, tested, and used in experiments. Some of the STIM-3B probes were found to have weakly adhering lead transfers, probably due to oxidation of the chromium underlayer used between the plated gold beams and the substrate. Improvements in the metal deposition procedures have been instituted to avoid the problem on future wafers. Measurements of access resistance have been shown to be helpful in identifying bad sites and will be automated during future characterization procedures. Access resistances are approximately 2.2kΩ for STIM-2B and 2.8kΩ for STIM-3B, with the latter higher due to the longer lead runs and beam lead transfers. Rapid thermal annealing has been shown to be effective in reducing the physical stress on probe shanks, producing more planar structures. The design and layout of STIM-2/-3 is also proceeding, and during the past term, the level shifters, polarity control circuitry, input data shift register, and site bias circuitry were all completed. The layout of these probes is expected to be completed during the coming term.

Work to complete the telemetry interface for the probes also made substantial progress during the past quarter. A new full-wave rectifier was designed. The circuitry produces both +5V and –5V regulated supplies from the RF carrier and is capable of sourcing and sinking 5mA load currents. The output resistance is about 30Ω, and the output voltages change less than ±150mV as the load resistance varies from 1kΩ to 1MΩ. Simulations show that the closed-loop regulator design can deliver the required regulated voltages at lower coil voltages (16V vs. 20.5V for open loop), making it preferable for our current process and allowing full 5mA output currents within the breakdown range of the fabricated devices.

During the coming term, work on STIM-2B/-3B development will be completed and these devices will be transferred to staff fabrication for application in-vivo. The design of STIM-2/-3 will be completed and these devices will enter fabrication. Finally, the design of the full telemetry interface for the stimulating probes will be completed and we will begin fabrication of the first leadless implantable stimulating probe structures.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0µA to ±254µA with a resolution of 2µA, while STIM-2 has a range from 0 to ±127µA with a resolution of 1µA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a

multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, work has proceeded in three areas. Additional STIM-2B and –3B probes have been fabricated, and the design, optimization, and layout of several additional circuit blocks for STIM-2 and –3 have also been completed. Most of the remaining circuit blocks needed for an RF-telemetry-based probe interface have also been designed and fully simulated. These will be fabricated using the 3µm UM BiCMOS process. The results in each of these areas are described more fully in the sections below.

2. Active Stimulating Probe Development

Recent active stimulating probe development has concentrated on completing the fabrication of new probes to facilitate the assembly of more 3D arrays. Unfortunately, a metal adhesion problem resulted in the loss of most of these devices. The 2D probes (without the plated beam lead transfers), which suffered much less from the adhesion problem. These probes have been tested, and the metal adhesion problem on the 3D devices has been investigated. We believe we have a solution in hand to complete more active 2D/3D probe wafers without the metal adhesion problem and move forward with the in-vivo application of the probes.

STIM-2B/3B

The development of the STIM-2B/3B probes is expected to yield very useful tools in the study of the central nervous system because of the large volume of tissue which these probes can instrument. These probes are quite simple and their function and design has been discussed extensively in previous quarterly reports.

The STIM-2B probe is the acute 2D version of this probe design, and it functions by simply clocking in 20 bits of data, which are used to select four of the available 64 sites. The addressed sites are connected via an analog multiplexer to input/output (I/O) pads that are driven from an external current source. A single flag bit is bundled with the site address; when it is set, the bit enables an on-chip amplifier that can be used for recording. STIM-3B is an extension of STIM-2B; it is altered to make it compatible with use in a 3D array. This includes the addition of outriggers with gold beam-lead interconnects and slotted wings which mate with micromachined spacers. A 4b register and second 4-channel analog multiplexer are added to allow addressing different probes

in a multi-probe 3D array. The 4b registers on the different probes are serially connected to reduce the overall number of leads required.

During the past quarter, we have completed additional active stimulating probes. From these probes, we have realized more of the acute 2D STIM-2B probes. In our testing protocol, we have also begun to track the resistance of every site of every channel during probing. This resistance is the sum of the PCB stalk, the probe multiplexing circuitry, and the shank leads. It does not include the site impedance. This resistance value is an important number that may help us understand the reason that an occasional site does not activate as well as others. Typical measurements of the site impedance done in saline solution include this as a series resistance. With this value known, we can more easily determine if a high impedance measurement is due to circuit or site problems. Typical STIM-2B and STIM-3B testing matrices are shown in Table 1 and Table 2, respectively. As expected, the STIM-3B probes have a somewhat higher resistance due to their longer lead paths, outriggers, and series-connected beam-leads.

Address\Site	Channel B															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	2.06k															
1		2.12k														
2			2.11k													
3				2.33k												
4					2.18k											
5						2.28k										
6							2.16k									
7								2.40k								
8									1.97k							
9										2.18k						
10											2.23k					
11												2.54k				
12													2.24k			
13														2.25k		
14															2.04k	
15																2.30k

Table 1: A typical STIM-2B probe test matrix with the measured circuit access resistance.

Unfortunately, we also encountered the adhesion problem mentioned above. The difficulty is one of poor adhesion of the electroplated gold beams to the underlying silicon dioxide and polysilicon as seen in Fig. 1. The gold is separating from the underlying 'adhesion promoting' layer of chromium as shown in Fig. 2. Because it is so unreactive, the adhesion of gold directly to SiO_2 and poly-Si is known to be poor; therefore, it is necessary to sputter a layer of highly-reactive material, such as chromium, underneath the gold to promote adhesion.

Address\Site				Channel B												
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	2.49k															
1		2.58k														
2			2.45k													
3				2.76k												
4					2.51k											
5						2.60k										
6							3.58k									
7								4.24k								
8									2.88k							
9										2.85k						
10											2.81k					
11												3.55k				
12													2.92k			
13														2.90k		
14															2.51k	
15																2.79k

Table 2: A typical STIM-3B probe test matrix with the measured circuit access resistance.

The gold-chromium adhesion problem has been noticed by several researchers in our laboratory recently. It is believed to be due to deposition of chromium oxide rather than unreacted chromium. It would be possible for this to happen if the chromium sputtering target is not 'pre-sputtered' long enough prior to opening the shutter to allow sputtering on the wafers to proceed. The 'pre-sputter' is necessary to remove any contaminants or any oxidized chromium that forms on the surface of the target while exposed to atmosphere. Because the pre-sputtering protocol has not changed recently, it is not likely that this is the cause of the current problem, although it may still be a contributing factor. There is also the possibility that some residual oxygen remains in our sputtering system chamber even after pumping down to base pressure. Because the inner surface of the chamber is coated with multiple layers of many different materials, it is possible for oxygen, usually in the form of water vapor, to become trapped in the materials and slowly release during sputtering. This possibility is exacerbated by the fact that our sputtering machine has a very large chamber that must be exposed to atmosphere every time a target or set of process wafers is changed. This allows water vapor to adsorb on the large inner surface area of the chamber. Since only a very thin layer (500Å) of chromium is deposited and the deposition rate is not very fast, it would not take a large source of oxygen to result in the conversion of significant amount of chromium to chromium oxide.

We believe that this problem is quite easily overcome by taking a few simple precautions. First, by increasing the 'pre-sputter' time, we can be sure to remove any oxidized chromium from the surface of the target. It appears possible to overcome the second possible failure source by allowing the sputtering chamber to pump down to its base pressure for a longer period of time. This is not ideal, since processing time in machines is at a premium, but it should greatly reduce any residual oxygen. A longer-term solution is to acquire a load-locked system.

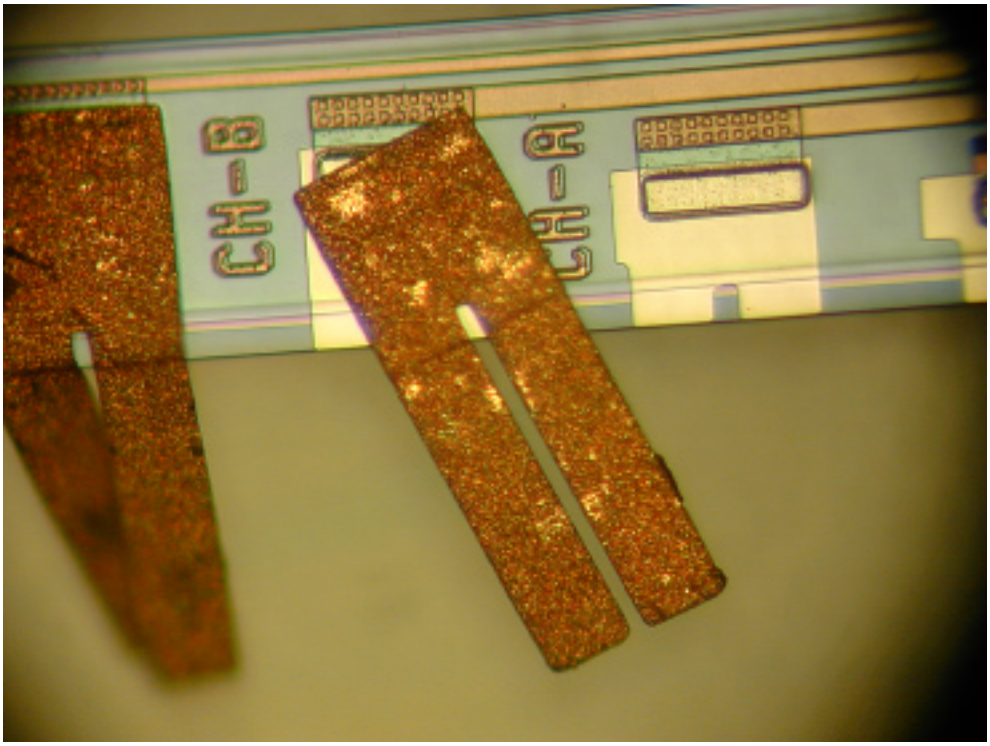

Fig. 1: The outrigger of a STIM-3B probe, showing the poor gold-to-chromium adhesion.

Performing a rapid thermal anneal (RTA) on the wafers 'after' the gold beam leads are in place is also a potential solution. This can be a difficult process since the gold-silicon eutectic is only 377°C. It is desirable to heat the wafers to as high as possible in order to allow the gold and chromium to intermix. The intermixing of these materials is limited, but nonetheless it would be important to stay below the gold-silicon eutectic. Several of the current probes that showed adhesion problems were annealed individually to see if adhesion could be improved. However, it was difficult to control the temperature to a relatively-low 350°C. Our RTA systems are designed to operate at much higher temperatures and are difficult to accurately control at such low temperatures. The tendency is to overshoot the target temperature. This actually results in improved contacts and adhesion because of interdiffusion of the gold with the underlying silicon. This is not a problem after the probes have been etched out because the only possible silicon-gold contact is in the contact regions and only then through the chromium. If the probes are still on the wafer, most of the beam-lead is in contact with bulk silicon where it overhangs the outrigger; however, even here contact would have to be through the chromium.

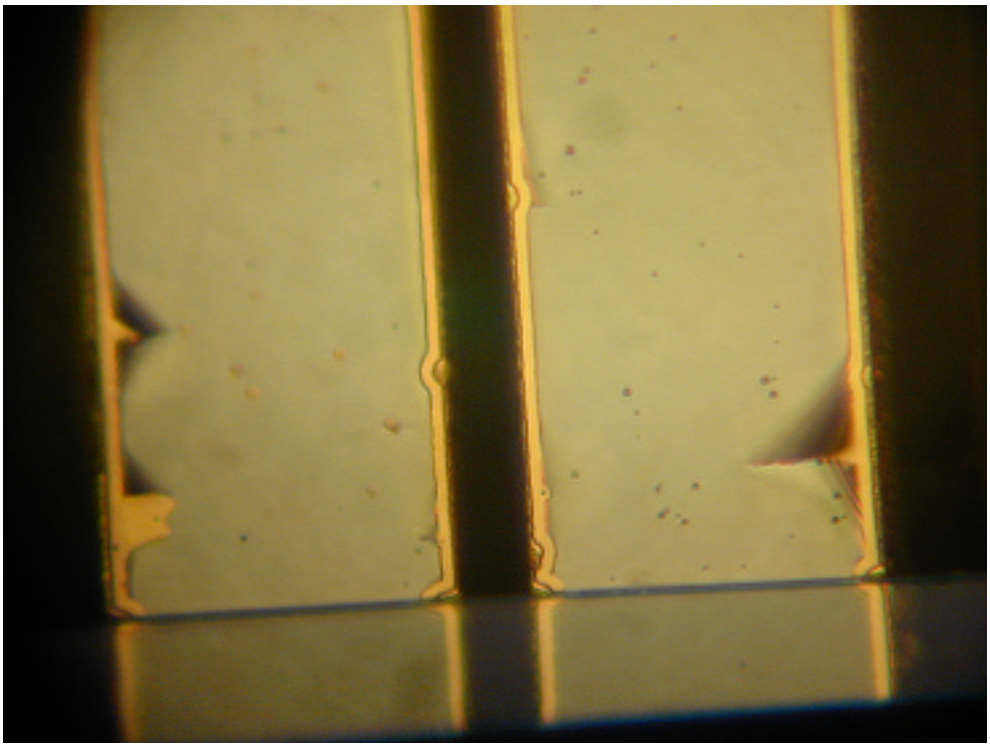

Fig. 2: The backside of a pair of electroplated gold beam-leads showing the chromium peeling loose. With good adhesion, this should not occur.

The recent RTA tests for adhesion did reveal one accidental, but interesting result. The shanks of the probes were initially not perfectly straight due to a mismatch in the stresses of the various layers. The same low temperature anneals used for treating the gold adhesion problem had the effect of reversing the curvature of the shanks. Increased time and temperature resulted in greater reversal of the curvature to the point where the probes could actually be curved the opposite direction. With proper control, this could be a very useful method of balancing the stress in the final devices in order to ensure that the probes are released with straight shanks. This effect is likely due to the anneal changing the stress in the LTO layer that covers the shank and circuit areas. It may also be helpful to anneal the LTO in order to densify the film and provide a better encapsulating layer.

During the coming quarter, we plan to complete the fabrication of several more wafers of the STIM-2B/3B probe design using better deposition procedures to eliminate the recent adhesion problems observed in these probes. We also believe that this simple probe design is a very good candidate to move into fabrication by our staff. We plan to lay out several variations of the STIM-2B/3B designs that will prove useful to neuro-physiologists so that these devices can begin to be used in everyday experiments. The main hurdle at this point is to reduce the overall width of the arrays so that they can be more easily used in experiments on common small animal models, such as the guinea pig. It may also be helpful to increase the length of the shanks to reach deeper structures.

One of the important issues that we have found in relation to the external system is the need to redesign our headstage circuitry and its package in such a way as to provide better visualization of the probe as it is being introduced into the neural tissue. Our use of the system has proven that the circuitry and its housing do not allow unobstructed visualization into the work area around the probe. We believe that we can shrink the physical size of the circuit and its enclosure to as little as one-third of its current size with the use of a commercially-fabricated fine-line multi-layer printed circuit board. The current prototype was fabricated in-house using a double-layer copper board with 250µm features and is therefore much larger than it could be. A carefully designed multi-layer PCB would also improve performance with relation to both noise and current-source output impedance. We plan to work toward this end in the coming quarter.

3. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

During the past quarter, final layout of STIM-2 has moved forward. Both the original STIM-2 and the redesigned STIM-2 use level shifters to shift the output DAC voltages from 0-5V to ±5V. As shown in Fig. 3, pmos transistors are responsible for overdriving the output voltage shift; thus, sufficient pmos W/L aspect ratios are needed for the circuit to operate correctly. We have re-simulated this circuit and have adjusted the W/L ratios to obtain improved performance. In the modified design, the pmos transistors have aspect ratio of (W/L=24/3), three times as that (W/L=7/3) of the output nmos transistors.

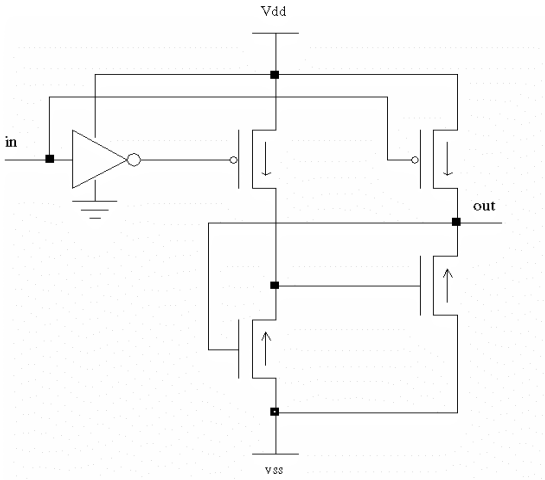

Fig. 3: Schematic of the level shifter used in STIM-2.

Source/sink control signal for the current DAC

Figure 4 shows a schematic for the polarity control circuit for the current DAC in the original STIM-2 design. This circuit controls whether the current-level specification is used for current sourcing or sinking. The different states are shown in Table 3. For the modified DAC design, the control circuit shown in Fig. 5 will be used, where the DAC

disable function is still maintained. The cst and dec1i signals (Figs. 4,5) come from an AND decoder of the clock strobe and the DAC_ select decoded signal.

Data signal for the current DAC

Figure 6 shows the circuit block that shifts the data signal from 0/5V to ±5V. This circuit remains unchanged in the modified design. When d7=1 (source on), the data lines d0~d6 will be inverted and level shifted; when d7=0 (sink on), they will only be level shifted.

DAC-enable	5V	5V	0V	0V
D7	5V	0V	5V	0V
sink_control	5V(sink off)	-5V(sink on)	5V(sink off)	5V(sink off)
source_control	5V(source on)	0V(source off)	0V(source off)	0V(source off)

Table 3: Functional states of the polarity control circuitry

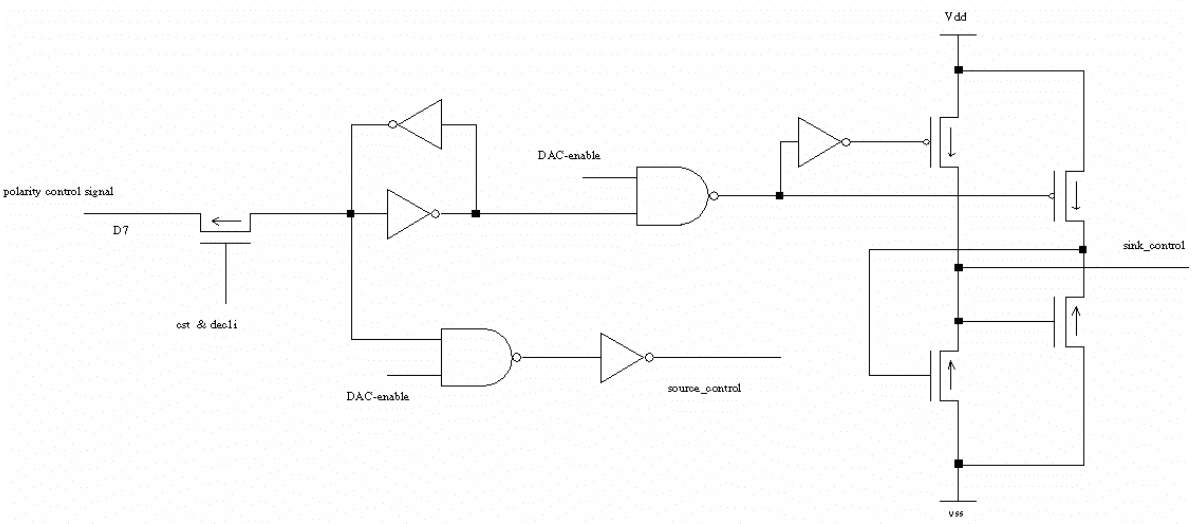

Fig 4: Schematic of the polarity control circuit of the original STIM-2 design

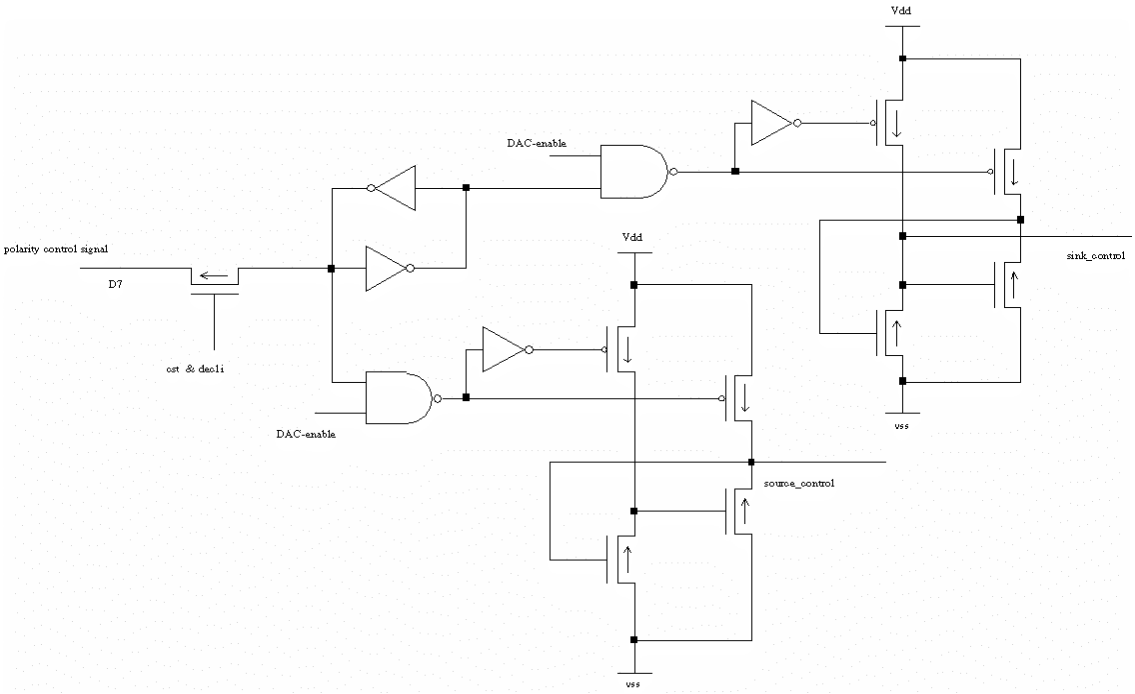

Fig. 5: Schematic of the polarity control circuit in the modified STIM-2 design

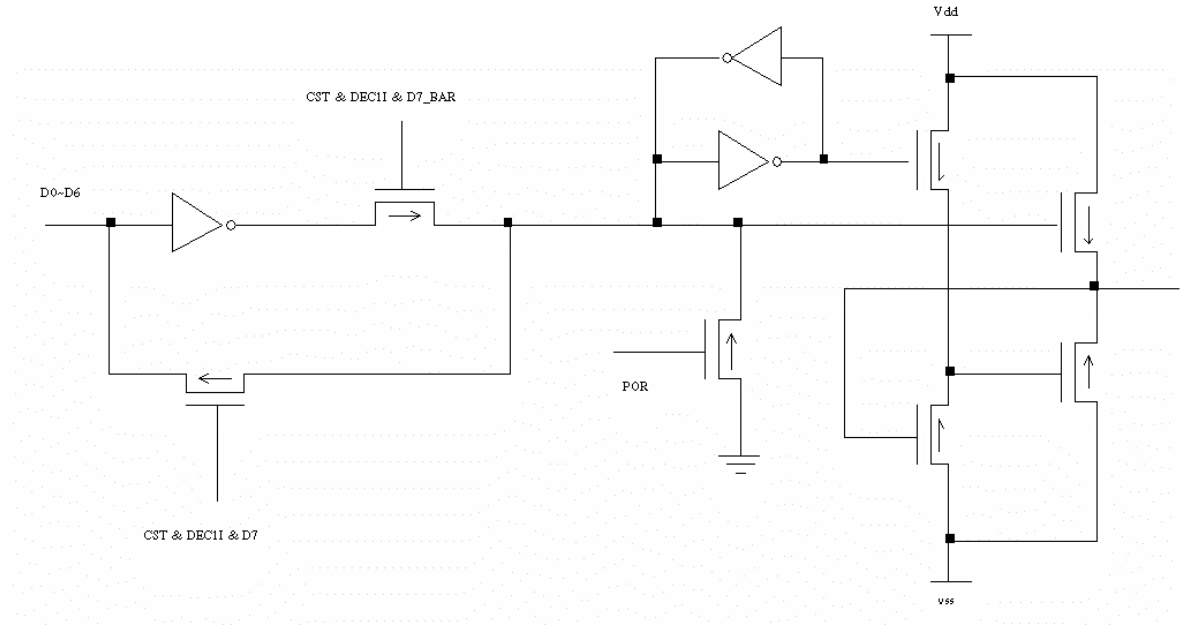

Fig. 6: Schematic of data signal circuit of STIM-2

Serial-to-parallel shift register

Figure 7 shows a single stage of the input data shift register. As defined by the data protocols in STIM-2, the first 8 bits of the serial input signal are latched by the data strobe for DAC/site selection. This circuitry has been re-simulated and optimized for use on the modified STIM-2 and STIM-3.

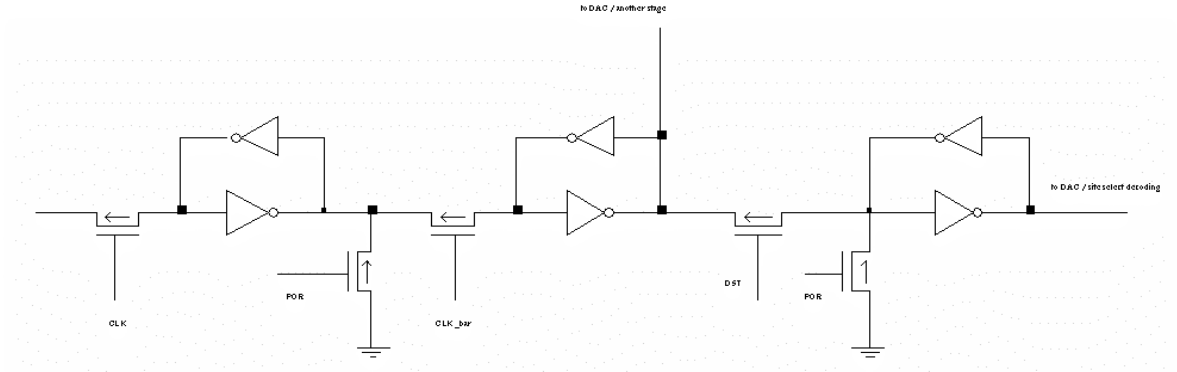

Fig. 7: Single stage of serial to parallel shift register

Site bias circuitry

The site bias circuit block for the original STIM-2 is shown in Fig. 8. The shunt_enable signal pulls the bias output to ground, grounding the unused sites between pulses. The anodic bias enable sets the output bias for unused sites at 0.6V. In the modified design, this block has been replaced by a voltage DAC producing 16 different bias voltages between –0.8V and +0.8V as programmed by the user.

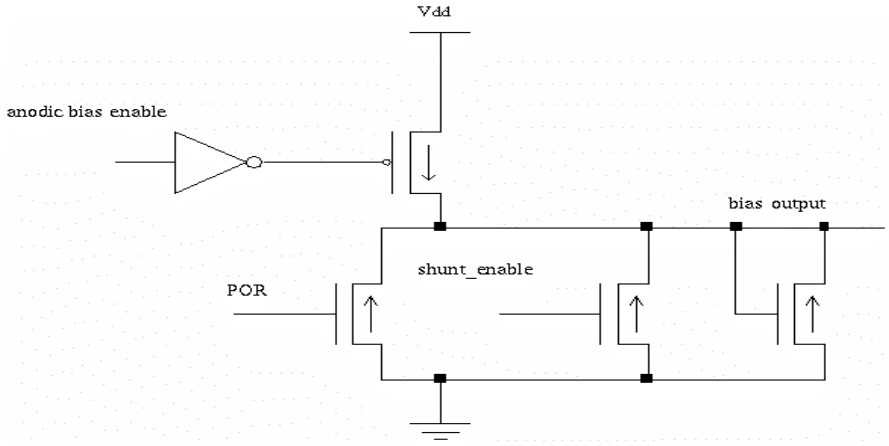

Fig. 8: Bias circuit in STIM-2

Output Site Interface

Figure 9 shows the circuit for interfacing with the sites at the front-end of the channel DACS. This circuitry must allow the various modes of the probe to be selected, including stimulating current calibration, site bias, and site impedance test. The site bias mode applies to inactive sites. In normal operation, the DAC output is simply routed through the series selection switch to the selected site. S1 is active in the special mode states representing the power-on-reset (POR), current calibration, impedance test, and recording modes. S2 is almost identical to S1, but excludes the recording mode, allowing

the AC signals from the test impedance and current calibration modes to pass directly to the output pad without passing through the amplifier. The output pad is now separate from the data pad to allow simultaneous stimulation and recording.

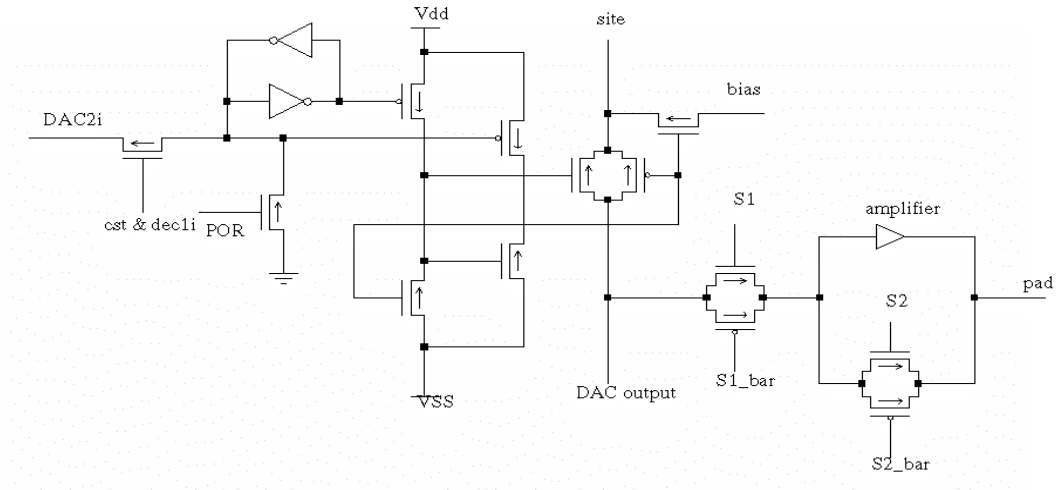

Fig. 9: Schematic of output interface circuitry for each site.

During the coming quarter, the redesign and layout for STIM-2 and STIM-3 will be completed and fabrication of these probes will begin.

4. A Telemetry-Powered CNS Stimulating System

In the previous quarterly report, test results and laboratory measurements on chips out of the first fabrication run were reported, and a series of changes and modifications were proposed to improve efficient power transfer. During the past quarter, these changes and modifications were made to the previously-designed circuit blocks, and simulations were carried out to verify the performance improvements and optimize the circuit characteristics. In addition to these changes, new versions of the regulator block were designed and simulated to achieve better performance.

A New Full-Wave Rectifier Design and Diode Characteristics:

The rectifier diodes are layed out ten times larger than the previously-characterized diodes to handle peak currents as high as 20mA to better serve the power consumption of the interface and stimulator chips. These diodes were tested individually on bonded chips using a HP4155 (Semiconductor Parameter Analyzer). Figure 10 shows these diodes with their assigned names. All these diodes are basically the same in layout and orientation. D1-D3 and D2-D4 are also the same with respect to circuit topology. The cross-section of these diodes is shown in Fig. 11. It is essentially that of a BJT transistor with base-collector terminals shorted.

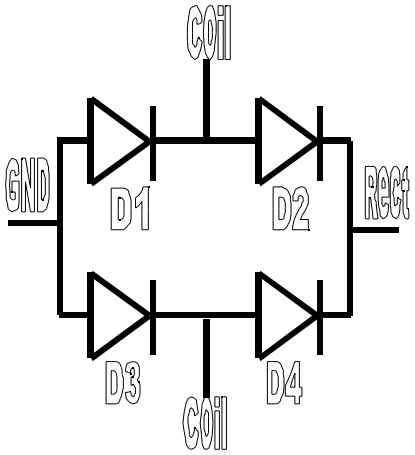

Fig. 10: Rectifier diode configuration

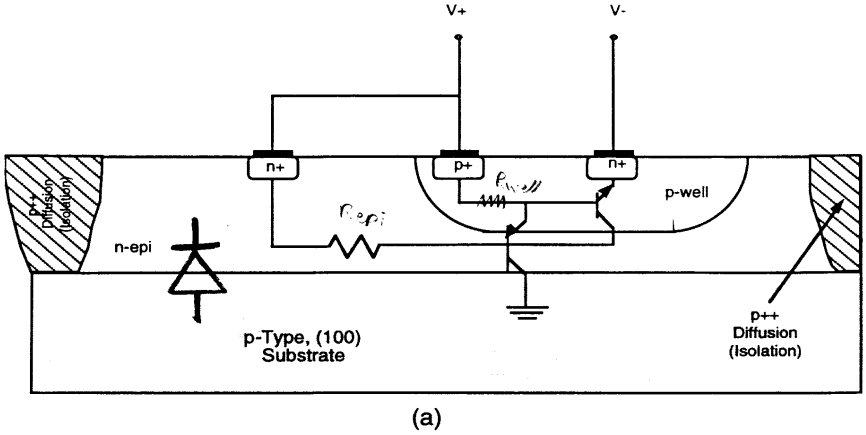

Fig. 11: The rectifier diode cross section

Figures 12 and 13 show D1 and D2 diodes when forward biased. It can be seen that D1 conducts more strongly than D2 and has much less parasitic resistance in series with it even though all the other parameters are the same. This is completely in agreement with our hypothesis and simulation results, which suggest that the alternating coil current passes through D2 and D4, which are the diodes between the p-well and the n-diffusion. But the current does not return back through D1 and D3 because the n-epi to p-well parasitic diodes D2 and D4 turn on at lower voltage (because of lower impurity concentration) and conduct much better (because of larger area) than D1 and D3. So these diodes do not let any current to pass through D1 and D3. Hence, Figs. 12 and 13 actually compare the forward conduction of the p-well-n-diffusion and n-epi:p-well diodes of D2 and D4, which are sufficient for full-wave rectification provided that the whole chip is isolated from the external common ground. To save chip area, D1 and D3 can be omitted in later designs and the actual full-wave rectifier is as shown in Fig. 14.

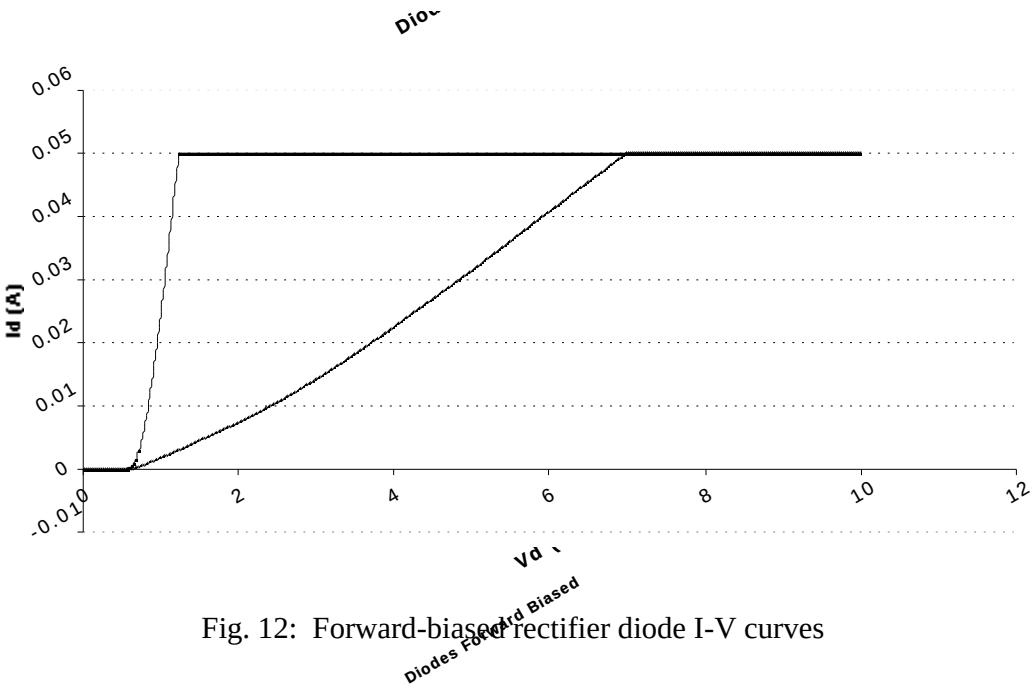

Fig. 12: Forward-biased rectifier diode I-V curves

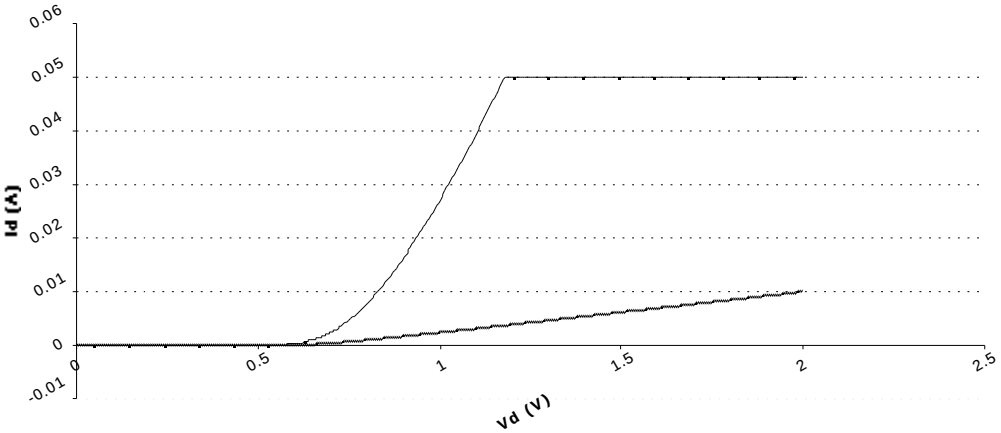

Fig. 13: Forward biased rectifier diode I-V curves (enlarged)

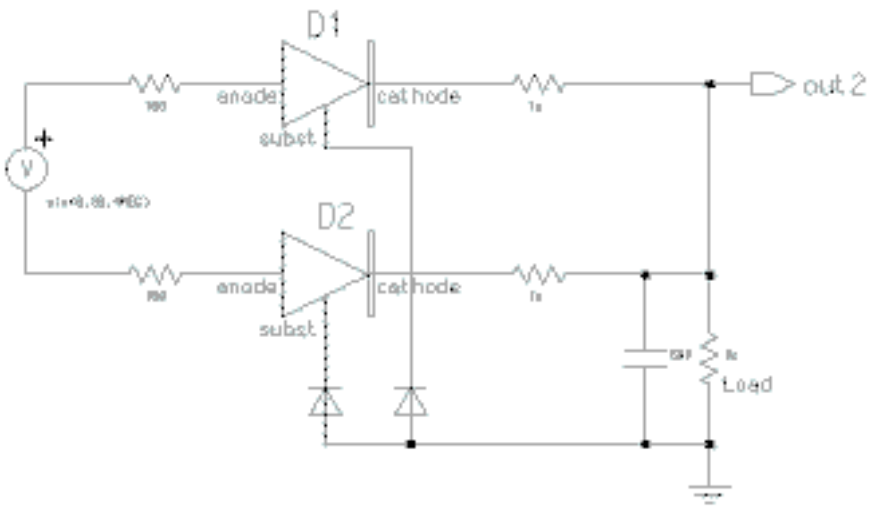

Fig. 14: Full wave rectifier using the n-epi:p-well parasitic diodes

Figures 15 and 16 compare the rectifier diodes when reverse biased. The reverse currents are almost the same at low voltages because D1 and its parasitic n-epi:p-well diode are in parallel. At large reverse voltages, D1 breaks down around 18V and D2 around 21V. This might be the main reason for high current consumption of the regulator at high input voltages. According to regulator simulations, coil voltages as high as $20V_{p\text{-}p}$ are enough for load currents less than 2mA, which is mostly the case. But higher load currents (5mA) for higher numbers of parallel stimulation currents would need more coil voltage. Slightly higher reverse breakdown voltages should be achievable by changing the impurity concentrations and processing parameters for high current stimulators.

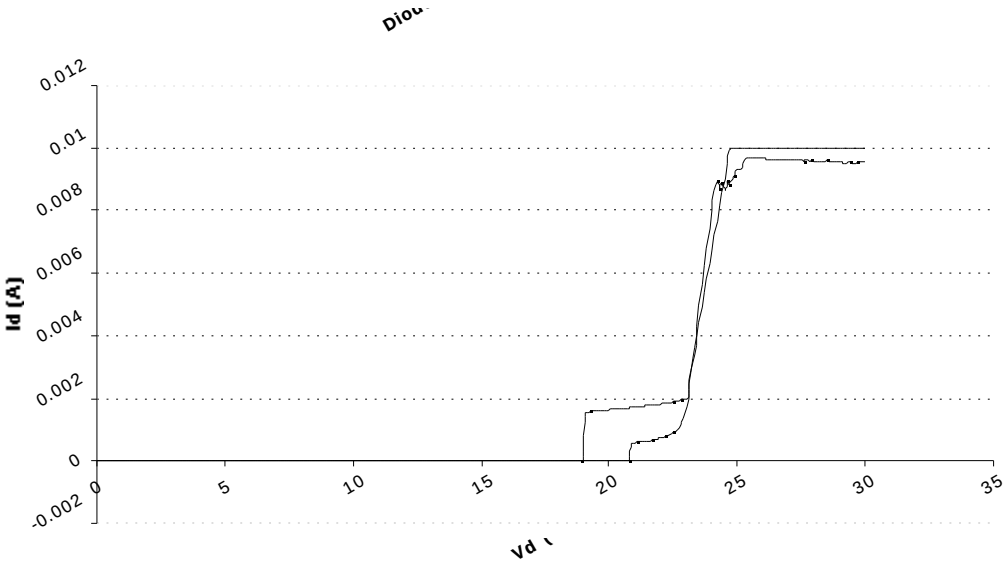

Fig. 15: Reverse-biased rectifier diode I-V curves

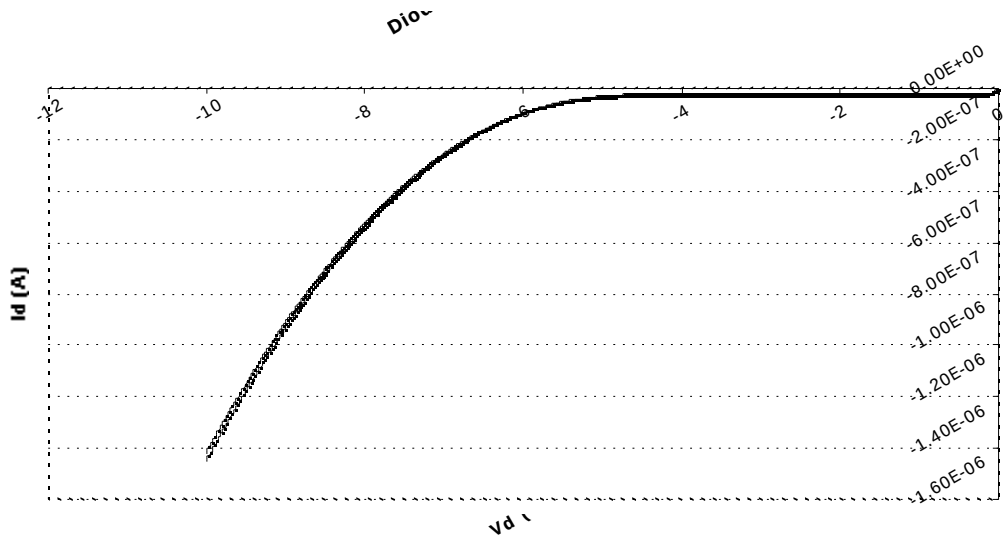

Fig. 16: Reverse-biased rectifier diode I-V curves (enlarged)

Class AB BiCMOS Unity Gain Buffer

One of the challenges in this part of the project is producing both regulated +5V and -5V supply voltages on a single chip. Two methods are proposed for this purpose:

1. Two separate regulators with a common ground generate +5V and –5V output voltages. These regulators use NPN and PNP pass transistors to source and sink the load currents, respectively.

2. A single regulator generates a +10V output. A +5V reference is applied to a unity-gain buffer, which is capable of both sourcing and sinking load currents. The next supplied chip, which is isolated from the interface uses the generated +10V, +5V and GND output terminals as +5V, GND and –5V, respectively.

The second approach was chosen for the present design because of the following reasons:

1. Each of the regulators in method 1 should have its own rectifier capacitor, which consumes a great deal of chip area.

2. The PNP transistors have very low current gain and poor characteristics in this process and their use should be eliminated.

3. Keeping a common ground layer (the substrate) and having voltages lower than ground on-chip gives rise to a number of complications and current leakage due to parasitic components.

4. The interface chip does not need to be integrated on the stimulating microprobes in the wireless CNS stimulating system. Hence, it can be easily isolated from the stimulator chip.

By choosing the 2nd method, the challenge is now to design a unity-gain buffer which is capable of sourcing as well as sinking 5mA of load current without significantly changing the regulated output voltages, i.e., it should have an extremely low output impedance. The simplest circuit for this purpose is a class B output stage. But because in this application the output should always stay around 5V, where the amplifier dead zone is, using a class AB output stage would be a better choice to keep the output ripple as low as possible. The use of PNP transistors should also be avoided as stated above. Accordingly, the PNP transistors in a regular class AB output stage were replaced by their PMOS-NPN counterparts as shown in Fig. 17. Furthermore, to reduce the required chip area, the PMOS biasing resistor was replaced by an NMOS transistor in the triode region. The final circuit schematic design is shown in Fig. 18.

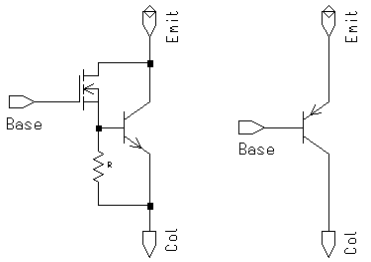

Fig. 17: BiCMOS PNP transistor equivalent using NMOS and NPN transistors

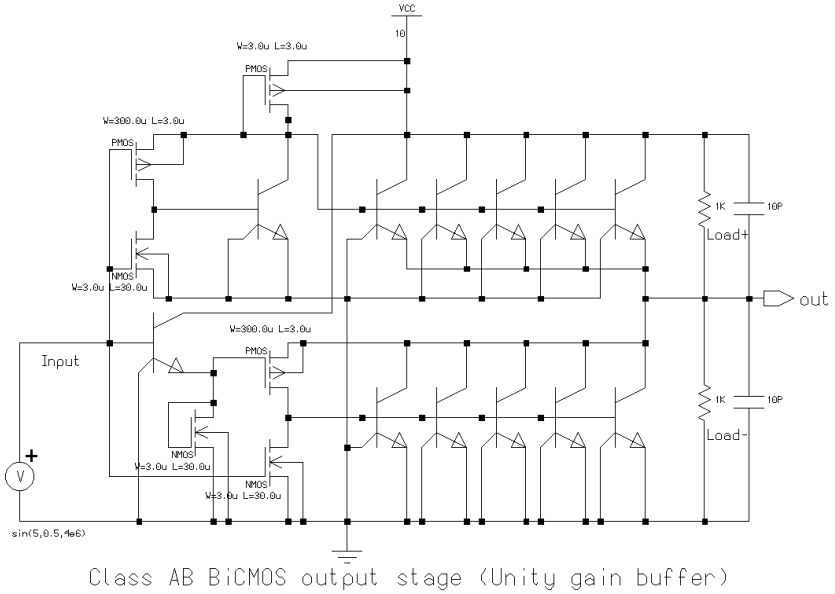

Fig. 18: BiCMOS unity-gain buffer schematic

The BiCMOS unity-gain buffer performance was simulated by separately changing each of the load+ and load- resistors over a wide range (1KΩ~1MΩ) and monitoring the change of output voltage. Figures 19 and 20 show that the output voltage does not change more than ±150mV over this range, which is equal to 30Ω of output resistance. This completely satisfies our purpose.

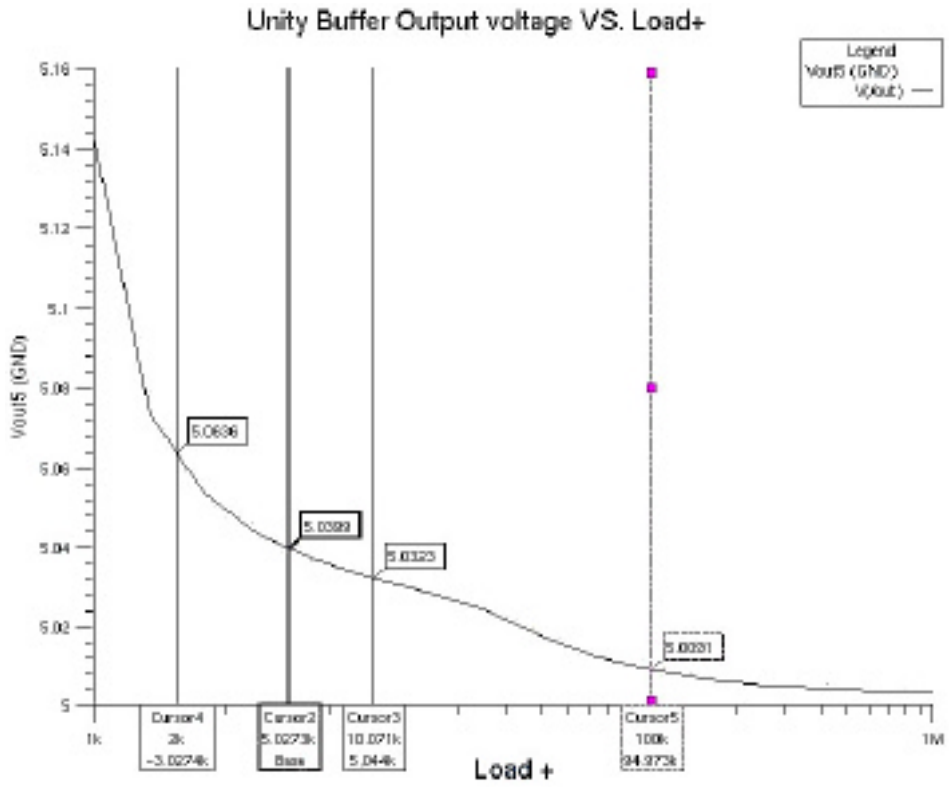

Fig. 19: BiCMOS unity-gain buffer output voltage while sinking current

Figure 21 shows a schematic design of the Modified Zener-Referenced Open-Loop Regulator. These are the major changes and modifications made to the previous open-loop regulator design (Regulator61), which was fabricated using the UM 3µm BiCMOS process. Test results were reported in the previous quarterly report.

1. The 10V output pass transistor is replaced by a Darlington pair to achieve higher current gain. Higher current gain reduces the base current, which is stolen from the Zener diode branch. This leads to lower power consumption by sending less current in to this branch for adequate biasing of the Zener diodes.

2. The 5V output pass transistor and Zener diode are omitted and both 10V and 5V reference voltages are taken from a single Zener diode branch acting as a voltage divider. This reduces the regulator power consumption significantly because the Zener diodes need more than 100µA to be appropriately biased by passing their knee point.

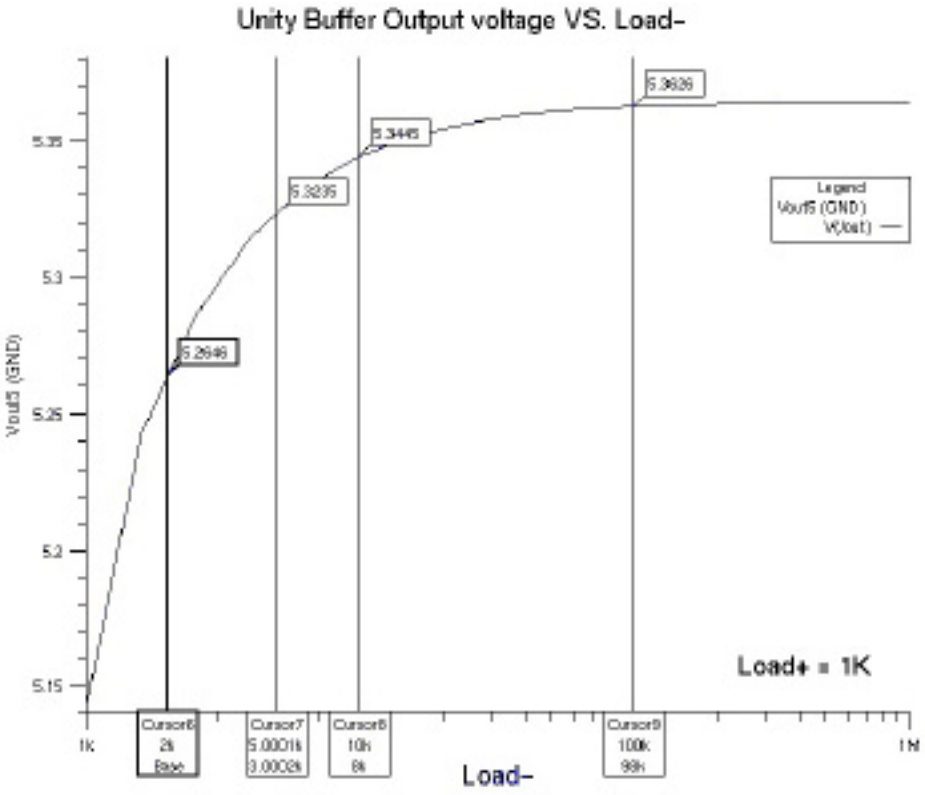

Fig. 20: BiCMOS unity gain buffer output voltage while sourcing current

3. The Zener diode geometries were changed from Z1A type to Z1B, which has shown a better performance by having a sharper knee point.

4. The previous start-up branch, which failed biasing the current source in many of the fabricated chips, is replaced by a more robust design. Cutting links are provided in both PMOS and NMOS parts to adjust the start-up voltage in case of any problem.

5. The four-diode full bridge rectifier is replaced by a two-diode version, utilizing their parasitic diodes as explained above in the “New Full-wave Rectifier design and Diode Characteristics” section.

6. A class AB BiCMOS unity-gain buffer is added to the 5V reference to generate a virtual ground for the stimulator chip.

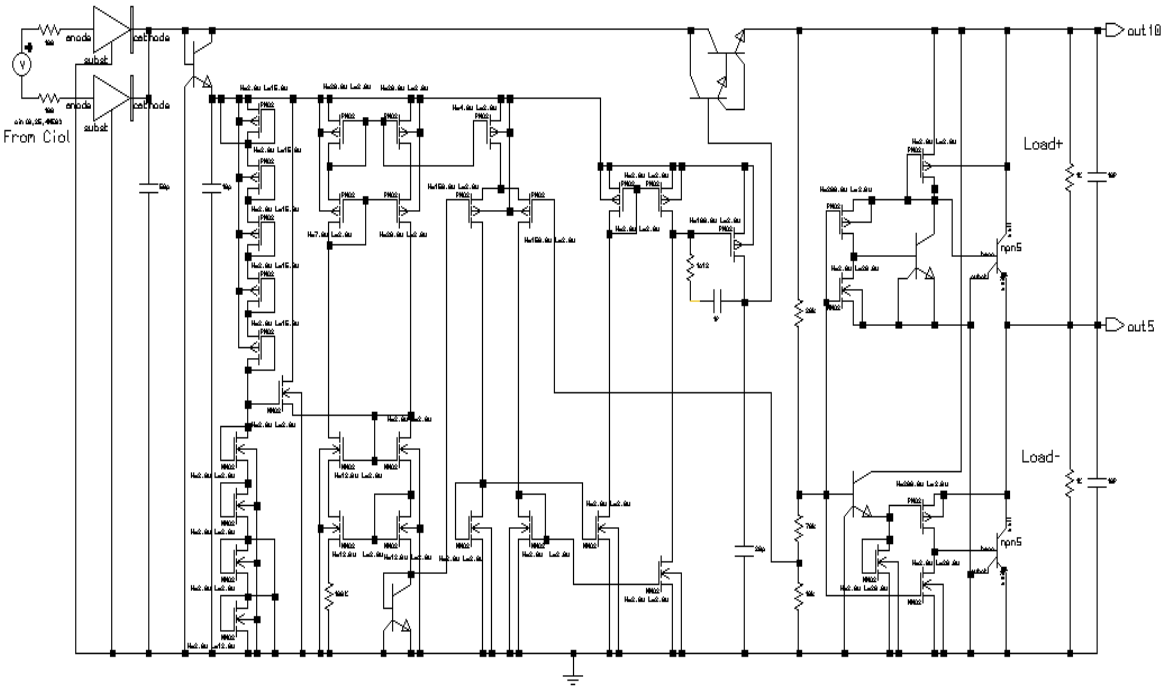

Fig. 21: Modified Zener-referenced open-loop regulator schematic (Regulator65)

Figure 22 shows the open-loop regulator DC response while sweeping its input voltage, i.e., the rectifier output voltage (V_{rect}), from 10V to 35V, which covers the range of coil voltages in this application. The curves shown, from top to bottom, are the start-up branch voltage, V_{be}, referenced current source, Zener branch biasing current, 10V output, and 5V output. These curves show that this 10V regulator starts regulation from input voltages as low as 12.5V and the outputs are maintained within the specified range very well.

Figure 23a shows the open-loop regulator transient response while supplying more than 5mA to each of the positive and negative 1kΩ loads, which is equal to 50mW of output power. The ripple is less than 5% on ±5V outputs, and the total current consumption is less than 150µA from the unregulated rectifier output. Figures 23b and 23c show the same waveforms while the Load- and Load+ are increased to 100KΩ, respectively. It can be seen that the output voltages have not changed significantly and are still in acceptable range.

Closed Loop Regulator Design:

All the previous regulator designs have been open loop, based on a Zener reference voltage. The advantages of these designs are higher frequency characteristics, lower component count, and smaller area on chip. But simulations show that the circuit performance can not be improved beyond a certain point because of the Zener diode non-

idealities and parasitic components. Another disadvantage of the Zener-referenced regulator is its high power dissipation because the Zener diodes need more than 100µA to pass their knee point.

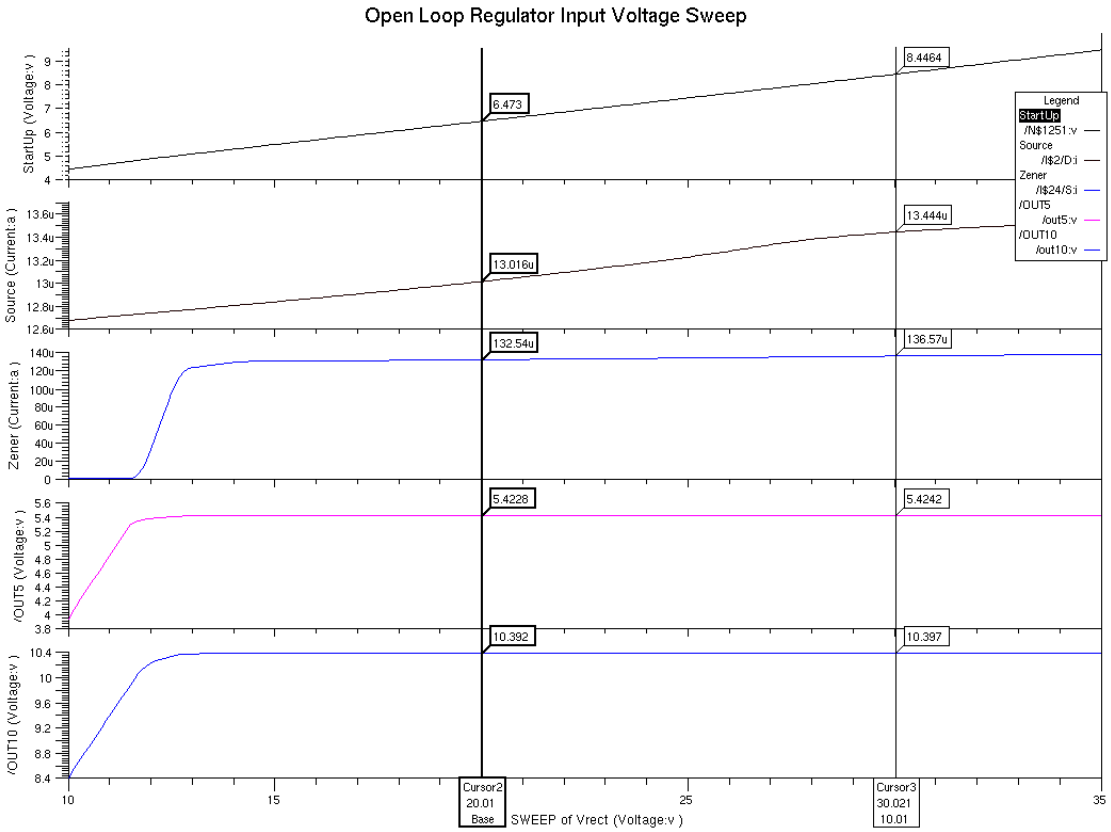

Fig. 22: The open-loop regulator input voltage sweep (V_{rect})

On the other hand, a closed-loop design actively suppresses the output regulator ripple and can compensate for parasitic components. Figure 24 shows the basic closed-loop regulator simplified schematic diagram. A major disadvantage of the closed-loop regulator is limited frequency response, which is mainly dictated by its op-amp. In this application, the carrier frequency is 4MHz, so the op-amp -3dB bandwidth should be at least 10MHz to effectively sense and suppress the 8MHz full-wave rectifier output ripple. To provide enough bandwidth for this regulator, an operational transconductance amplifier (OTA) was utilized in this design.

The closed-loop regulator schematic diagram is shown in Fig. 25. To decrease power consumption, a single diode-connected BJT is used to generate one V_{be} voltage drop as the reference voltage. This diode is used in a supply-independent V_{be}-referenced current source as well to provide required biasing voltages for the OTA. To cover common input voltage ranges (CMR) as low as 0.7V, PMOS transistors are selected for the OTA differential input stage.

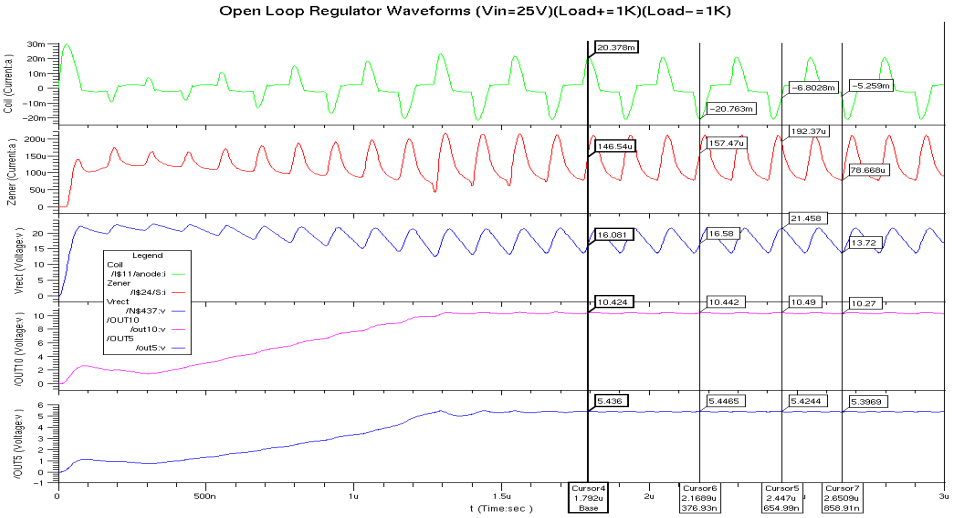

Fig. 23a.

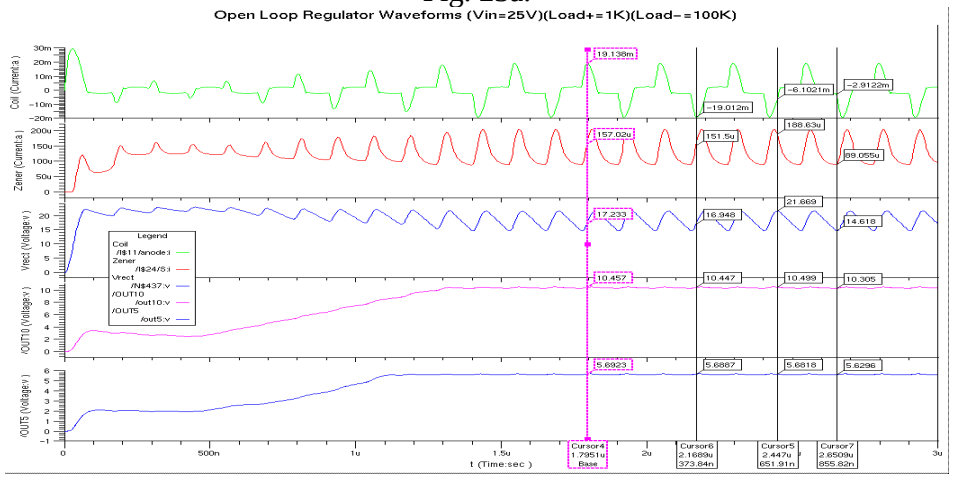

Fig. 23b.

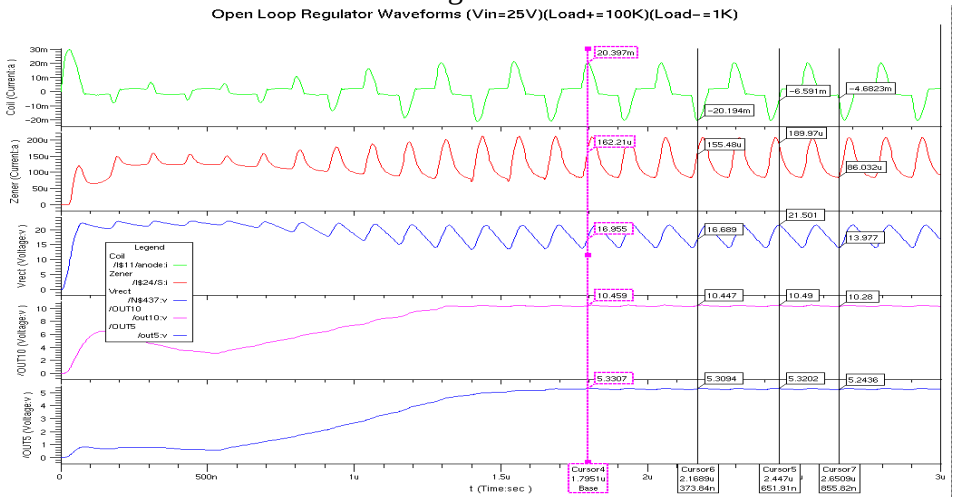

Fig. 23c: The open-loop regulator transient waveforms

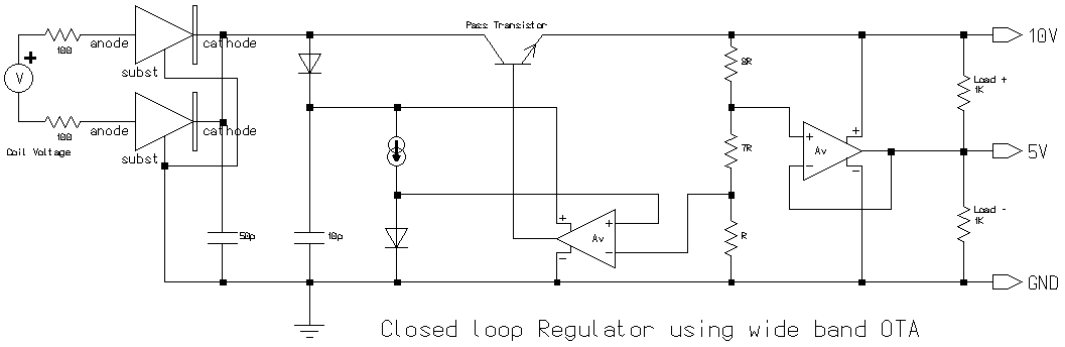

Fig. 24: Closed-loop regulator simplified schematic diagram

OTAs are primarily used to drive capacitive loads, but here a BJT pass transistor should be driven as the load, so a source follower buffer has been added to the OTA to make it capable of supplying base current. Current gain of the UofM BiCMOS BJTs are between 80-100, which means more than 100µA of base current is needed to pass 10mA of regulated current. This is too high for the OTA buffer, so the BJT pass transistor was replaced by a Darlington pair to decrease the required base current. A resistive voltage divider feeds back a small portion of the output voltage (0.7/10V) to the OTA negative input. The output voltage can be easily adjusted to the desired value by changing the resistor values. Cutting links can be added to the regulator layout to fine-tune the regulator voltage after fabrication. This resistive voltage divider branch can be connected to the OTA buffered output before or after the pass transistor and passes 61µA to ground for a 10V output. According to simulations, the former case leads to higher bandwidth but the latter case has the advantage of lower OTA power consumption and gives less output ripple.

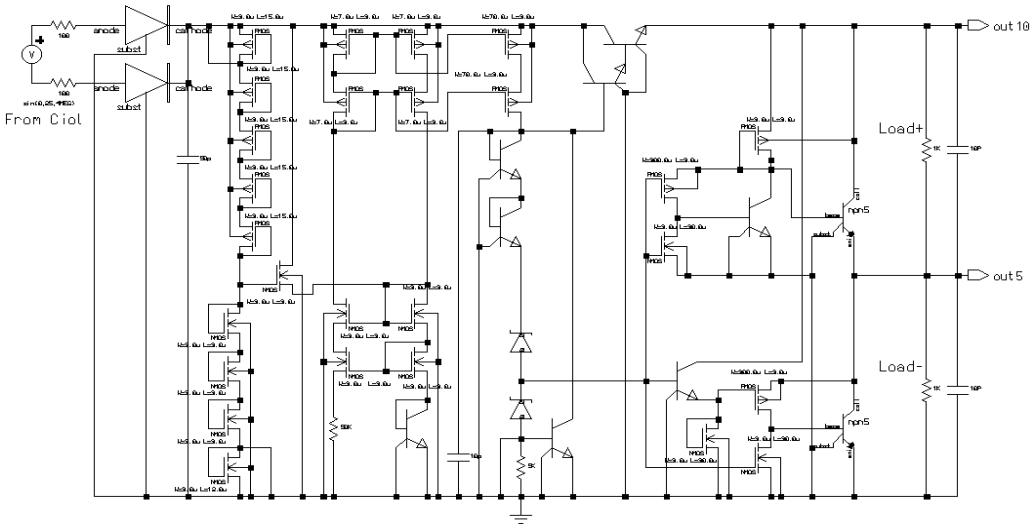

Fig. 25: Closed-loop regulator schematic (Regulator42)

Since the OTA supply voltage ripple directly shows up on its output at high frequency (poor PSRR at high frequency) and finally affects the regulator output ripple percentage, a separate unregulated supply is provided by means of a diode and a 10pF capacitor after the rectifier block. The diode isolates the OTA supply voltage from the rectifier ripple as long as the OTA power consumption is kept low. This voltage varies with the rectifier voltage (V_{rect}) peak value but the currents passing through the OTA branches are all controlled by the supply-independent current source, so they do not change significantly.

Figure 26 shows the closed-loop regulator DC response while sweeping its input voltage, i.e., the rectifier output voltage (V_{rect}), from 10V to 40V, which covers the range of coil voltages in this application. The curves shown, from top to bottom, are the start-up branch voltage, V_{be}, the referenced current source, differential amplifier branch current, the 5V output, and the 10V output. These curves show that this 10V regulator starts regulation from input voltages as low as 12V and the outputs are maintained very close to the specified values, especially in 12V~25V input voltage range. The absence of the Zener diode voltage references in this design has decreased the current consumption significantly.

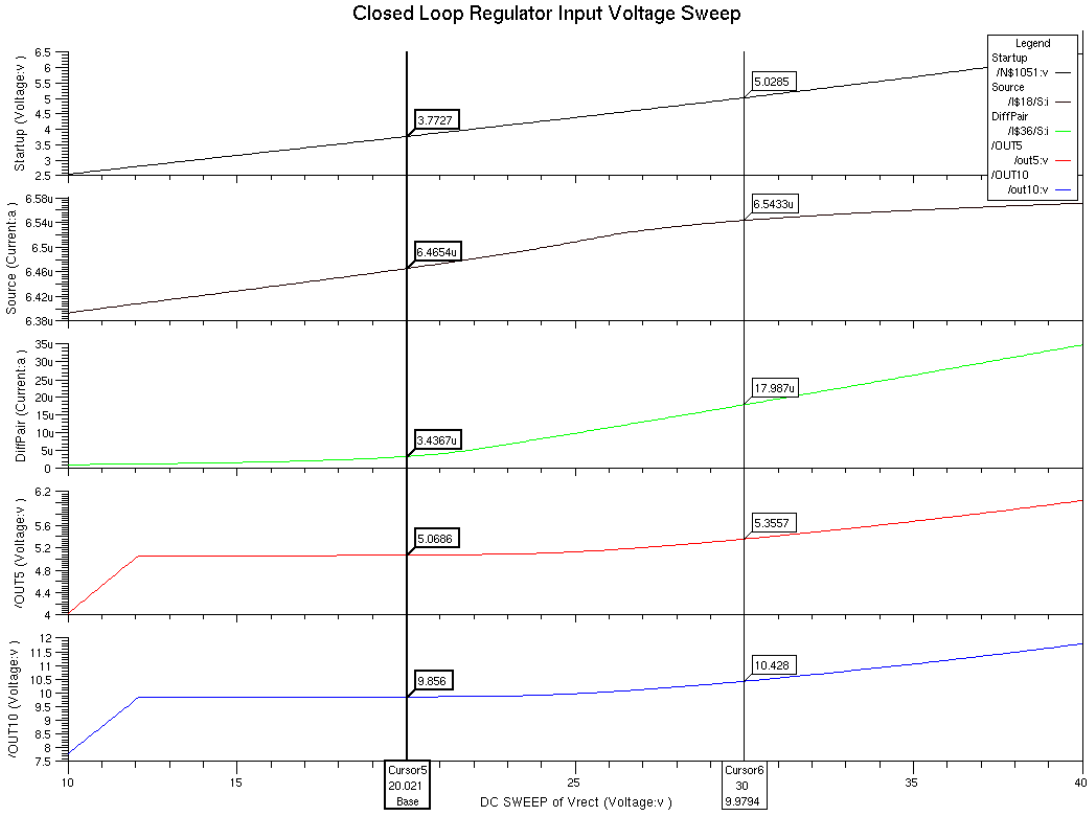

Fig. 26: The closed-loop regulator input voltage sweep (V_{rect})

Figure 27a shows the closed-loop regulator transient response while supplying more than 5mA to each of the positive and negative 1kΩ loads. The ripple is less than 5% on ±5V outputs, and the total current consumption is only about 65µA. Figures 27b and 27c show the same waveforms, while the Load- and Load+ are increased to 100KΩ, respectively. It can be seen that the output voltages have not changed significantly and are still in acceptable range. The only disadvantages of this new design compared to the open-loop design are larger area and more sensitivity to process parameter variation, which can be eliminated by providing cutting links to adjust branch currents and output voltages.

Simulation results for the three different regulator designs are compared in Table 4 to 6. Reg62 is the first open-loop design, which is now fabricated and tested. Reg65 is the improved version of the open loop regulator, and Reg42 is the closed-loop regulator design, which is shown in Fig. 25 and discussed above.

Table 4: Regulator performance with: $V_{in(p-p)}$=30V R_L=1KΩ V_0=10V R_{coil}=200Ω

Regulator	**V_{omax}(V)**	**V_{omin}(V)**	**V_{oDC}(V)**	**%Ripple**	**Current Consumption(_µA)**
Reg62	7.05	5.35	6.2*	%27	400
Reg65	5.6	5.05	5.3*	%10	170
Reg42	10	9.8	9.9	%2	70

* Regulators 62 and 51 fail to give 10V output with this load current.

Table 5: Regulator performance with: $V_{in(p-p)}$=30V R_L=2KΩ V_0=10V R_{coil}=200Ω

Regulator	**V_{omax}(V)**	**V_{omin}(V)**	**V_{oDC}(V)**	**%Ripple**	**Current Consumption(µA)**
Reg62	10.24	9.24	9.74	%10.3	200
Reg51	9.54	9.04	9.29	%5.4	150
Reg41	10.1	9.97	10.03	%1.3	65

Table 6: Regulator performance with: $V_{in(p-p)}$=20.5V R_L=2KΩ V_0=10V R_{coil}=200Ω

Regulator	**V_{omax}(V)**	**V_{omin}(V)**	**V_{oDC}(V)**	**%Ripple**	**Current Consumption(µA)**
Reg62	10.24	8.66	9.45	%16.7	200
Reg65	9.48	8.98	9.23	%5.4	100
Reg42	9.92	9.60	9.76	%3.3	30

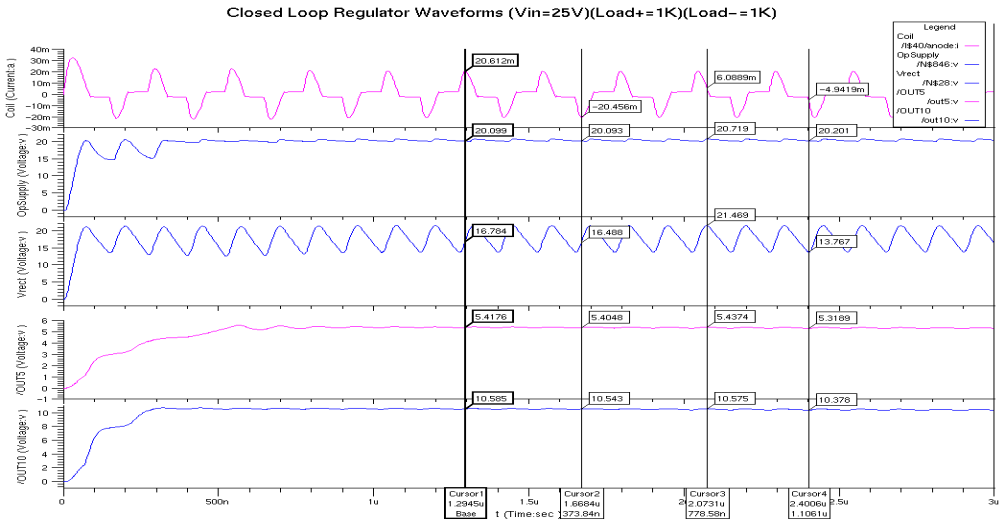

Fig. 27a.

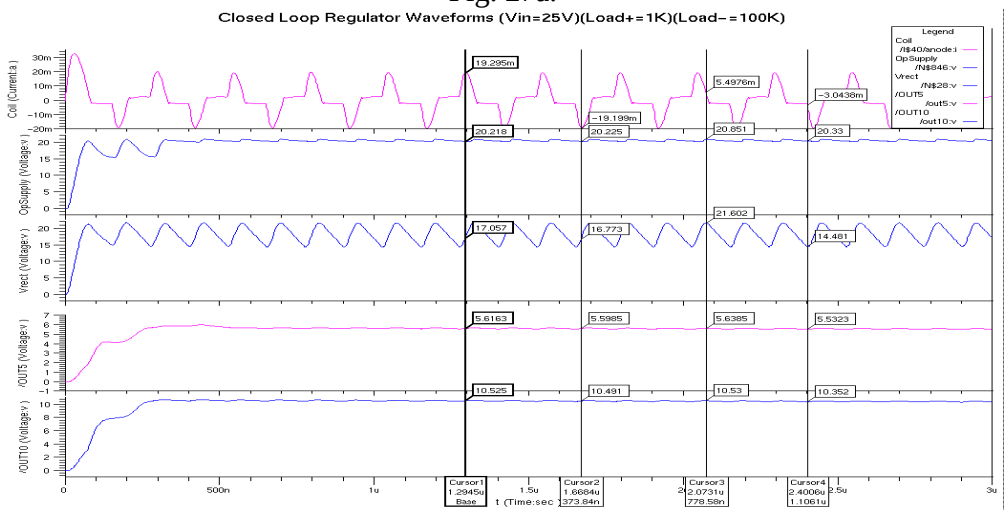

Fig. 27b.

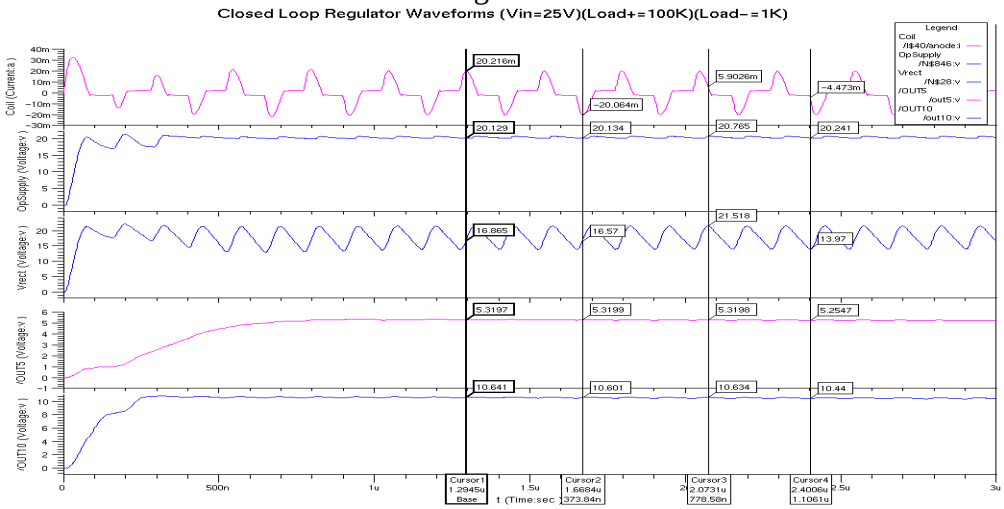

Fig. 27c: The closed-loop regulator transient waveforms

Simulations also show that the closed-loop regulator design can generate regulated output a with minimum input voltage of 16V(p-p) but open loop regulators fail to give regulated output with less that 20.5V(p-p) input coil voltage. This parameter (minimum p-p coil voltage) is very important because rectifier diode DC tests showed that their breakdown voltage is around 20V, which is less that the open loop regulator minimum input voltage for supplying 5mA. So with high load currents, using closed-loop regulators might be the only way to generate regulated output voltages as high as 10V. Table 7 summarizes minimum coil voltage required to generate closed-loop regulated 10V output with different loads.

Table 7: Closed-loop regulators performance minimum required coil voltage with different loads.

R_L (KΩ)	$V_{coil\text{-}min\text{-}p\text{-}p}$ (V)	$V_{rectify}$(V)	V_{out}(V)	V_{oDC}(V)	%Ripple
1	28	11.45~23.33	9.72~9.99	9.85	2.7%
2	20.5	10.66~17.27	9.60~9.92	9.76	3.3%
5	16	10.61~13.62	9.65~10.1	9.87	4.6%

Next quarter plans:

During the next quarter, the above regulator designs will be laid out as individual blocks and prepared for the next UofM 3µm BiCMOS run. The digital block for the interface chip will be designed and simulated, which consists of the timing, strobe generating, and command shift register circuits. The digital block will be laid out and put together with other available blocks (regulator, clock recovery, and envelope detector) to fabricate the first version of a complete telemetry interface chip.

5. Conclusions

During the past quarter, work has progressed in several areas. Additional STIM-2B/-3B probes were processed to completion. Several of the STIM-2B probes were mounted, tested, and used in experiments. Some of the STIM-3B probes were found to have weakly adhering lead transfers, probably due to oxidation of the chromium underlayer used between the plated gold beams and the substrate. Improvements in the metal deposition procedures have been instituted to avoid the problem on future wafers. Measurements of access resistance have been shown to be helpful in identifying bad sites and will be automated during future characterization procedures. Access resistances are approximately 2.2kΩ for STIM-2B and 2.8kΩ for STIM-3B, with the latter higher due to the longer lead runs and beam lead transfers. Rapid thermal annealing has been shown to be effective in reducing the physical stress on probe shanks, producing more planar structures. The design and layout of STIM-2/-3 is also proceeding, and during the past term, the level shifters, polarity control circuitry, input data shift register, and site bias

circuitry were all completed. The layout of these probes is expected to be completed during the coming term.

Work to complete the telemetry interface for the probes also made substantial progress during the past quarter. A new full-wave rectifier was designed. The circuitry produces both +5V and –5V regulated supplies from the RF carrier and is capable of sourcing and sinking 5mA load currents. The output resistance is about 30Ω, and the output voltages change less than ±150mV as the load resistance varies from 1kΩ to 1MΩ. Simulations show that the closed-loop regulator design can deliver the required regulated voltages at lower coil voltages (16V vs. 20.5V for open loop), making it preferable for our current process and allowing full 5mA output currents within the breakdown range of the fabricated devices.

During the coming term, work on STIM-2B/-3B development will be completed and these devices will be transferred to staff fabrication for application in-vivo. The design of STIM-2/-3 will be completed and these devices will enter fabrication. Finally, the design of the full telemetry interface for the stimulating probes will be completed and we will begin fabrication of the first leadless implantable stimulating probe structures.